

ATTORNEY DOCKET NO.:
017575.0551 (TAMUS 1539)

PATENT APPLICATION

09/997,786

2858



1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

RECEIVED
MAR 23 2002
2800 MAIL ROOM

In re Application of: Duncan M. Walker, et al.
Serial No.: 09/997,786
Filing Date: November 30, 2001
Confirmation No. 4798
Title: SYSTEM AND METHOD FOR DETECTING
QUIESCENT CURRENT IN AN INTEGRATED
CIRCUIT

Assistant Commissioner for Patents
Washington, D.C. 20231

I hereby certify that this communication is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231.

R. Cisneros de Chaves

Date: March 25, 2002

Dear Sir:

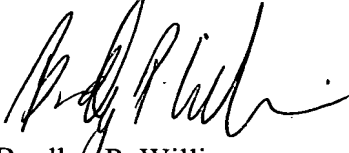
INFORMATION DISCLOSURE STATEMENT

Applicants respectfully request, pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, that the references listed on the attached PTO-1449 form be considered and cited in the examination of the above-identified patent application. Copies of these references are enclosed for the convenience of the Examiner. Furthermore, pursuant to 37 C.F.R. § 1.97(g) and (h), no representation is made that a search has been made or that these references qualify as prior art or that these references are material to the patentability of the present application.

This Information Disclosure Statement is being submitted before an Office Action on the merits, and therefore, pursuant to 37 C.F.R. § 1.97(b), no fee is believed due. However, the Commissioner is hereby authorized to charge any required fee to Deposit Account No. 02-0384 of Baker Botts L.L.P.

Respectfully submitted,

BAKER BOTTS L.L.P.
Attorneys for Applicants

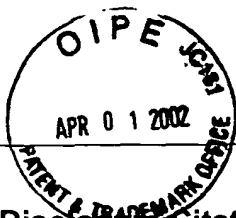


Bradley P. Williams
Reg. No. 40,227

Please Send Correspondence to:

Bradley P. Williams, Esq.
Baker Botts L.L.P.
2001 Ross Avenue, Suite 600
Dallas, TX 75201-2980
Tel. 214.953.6447
Fax. 214.661.4447
brad.williams@bakerbotts.com

Date: March 25, 2002



PTO-1449		Application No. 09/997,786		Applicant(s) Duncan M. Walker, et al.			
Information Disclosure Citation in an Application		Docket Number 017575.0551		Group Art Unit		Filing Date 11/30/2001	
U.S. PATENT DOCUMENTS							
		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	A	4,677,380	06/30/1987	Popovic et al	324	252	06/07/1983
	B	5,570,034	10/29/1996	Needham et al.	324	763	12/29/1994
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
	C						YES NO
	D						
NON-PATENT DOCUMENTS							
		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)					DATE
	E	J. Lin and M. Milkovic, "Performance Limitations of Stochastic Sensors," <u>Midwest Symposium on Circuits and Systems</u>					Aug. 1992
	F	P. Nigh, W. Needham, K. Butler, P. Maxwell and R. Aitken, "An Experimental Study Comparing the Relative Effectiveness of Functional, Scan, IDDq and Delay-fault Testing, <u>IEEE Int'l ASIC Conference</u>					1996
	G	J. Rius and J. Figueras, "Dynamic Characterization of Built-In Current Sensors Based on PN Junctions: Analysis and Experiments," <u>Journal of Electronic Testing: Theory and Applications</u> , Vol. 9, No. 3					Dec. 1996
	H	J.M. Soden and C.F Hawkins, "IDDQ Testing and Defect Classes - A Tutorial," <u>IEEE Custom Integrated Circuits Conference</u>					1995
	I	K.M. Wallquist, "On the Effect of ISSQ Testing in Reducing Early Failure Rate," <u>IEEE Int'l Test Conference</u>					1995
	J	T.R. Henry and T. Soo, "Burn-In Elimination of a High Volume Microprocessor Using IDDQ," <u>IEEE Int'l Test Conference</u>					1996
	K	T.W. Williams, R. Kapur, M.R. Mercer, R.H. Dennard and W. Maly, "Iddq Test: Sensitivity Analysis of Scaling, <u>IEEE Int'l Test Conference</u>					1996
	L	D.M.H. Walker, "Requirements for Practical IDDQ Testing of Deep Submicron Circuits," <u>IEEE Int'l Workshop on Defect Based Training</u>					April 2000
	M	P.C. Maxwell, R.C. Aitken, K.R. Kollitz and A.C. Brown, "IDDQ and AC Scan: The War Against Unmodelled Defects," <u>IEEE Int'l Test Conference</u>					1996
	N	T. Meneghini and D. Josephson, "IDDQ Testing of a 180MHz HP PA-RISC Microprocessor with Redundancy Programmed Caches," <u>IEEE Int'l Workshop on IDDQ Testing</u>					Nov. 1997
	O	P. Nigh, D. Vallett, A. Patel and J. Wright, "Failure Analysis of Timing and IDDq-only Failures from the SEMATECH Test Methods Experiment," <u>IEEE Int'l Test Conference</u>					1998
	P	T.A. Unni and D.M.H. Walker, "Model-Based IDDQ Pass/Fail Limit Setting, <u>IEEE Int'l Workshop on IDDQ Testing</u>					Nov. 1998
	Q	A.E. Gattiker and W. Maly, "Current Signatures: Application," <u>IEEE Int'l Test Conference</u>					1997
	R	C. Thibeault, "On the Comparison of ΔI_{DDQ} and I_{DDQ} Testing," <u>IEEE VLSI Test Symposium</u>					April 1999
EXAMINER				DATE CONSIDERED			
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.							

U.S. Patent and Trademark Office



PTO-1449		Application No. 09/997,786		Applicant(s) Duncan M. Walker, et al.			
Information Disclosure Citation in an Application		Docket Number 017575.0551		Group Art Unit	Filing Date 11/30/2001		
U.S. PATENT DOCUMENTS							
		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	A						
	B						
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES NO
	C						
NON-PATENT DOCUMENTS							
		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)					DATE
	D	C. Thibeault, "An Histogram Based Procedure for Current Testing of Active Defects," <u>IEEE Int'l Test Conference</u>					1999
	E	A.C. Miller, "IDDQ Testing in Deep Submicron Integrated Circuits," <u>IEEE Int'l Test Conference</u>					1999
	F	P. Maxwell, P. O'Neill, R. Aitken, R. Dudley, N. Jaarsma, M. Quach and D. Wiseman, "Current Ratios: A Self-Scaling Technique for Production IDDQ Testing," <u>IEEE Int'l Test Conference</u>					1999
	G	S. Jandhyala, H. Balachandran, S. Menon and A. Jayasumana, "Clustering Based Identification of Faulty ICs Using I_{DDQ} Tests," <u>IEEE Int'l Workshop on IDDQ Testing</u>					Nov. 1998
	H	S. Jandhyala, H. Balachandran, A.P. Jayasumana, "Clustering Based Techniques for I_{DDQ} Testing," <u>IEEE Int'l Test Conference</u>					1999
	I	S. Hentschke, S. Rohrer and N. Reifschneider, "Stochastic Magnetic Field Micro-Sensor," <u>IEEE Int'l ASIC Conference</u>					1996
	J	J.P.M. van Lammeren, " I_{CCQ} : a Test Method for Analogue VLSI Based on Current Monitoring," <u>IEEE Int'l Workshop on IDDQ Testing</u>					1997
	K	K. Nose and T. Sakurai, "Micro IDDQ Test Using Lorentz Force MOSFET's," <u>IEEE Symposium on VLSI Technology</u>					1999
	L	F.J. Kub and C.S. Scott, "Multiple-Gate Split-Drain MOSFET Magnetic-Field Sensing Device and Amplifier," <u>International Electron Devices Meeting</u>					1992
	M	H.-M. Yang, Y.-C. Huang, T.-F. Lei, C.-L. Lee and S.-C. Chao, "High-resolution MOS Magnetic Sensor with Thin Oxide in Standard Submicron CMOS Process," <u>Sensors and Actuators</u> , Vol. A57					1996
	N	J.W.A. von Kluge and W.A. Langheinrich, "An Analytical Model of MAGFET Sensitivity Including Secondary Effects Using a Continuous Description of the Geometric Correction Factor G," <u>IEEE Transactions on Electron Devices</u> , Vol. 46, No. 1					Jan. 1999
	O	S. Hentschke, "Digital Stochastic Magnetic-Field Detection," <u>Sensors and Actuators</u> , Vol. A57					1996
	P	H.J.M. Veendrick, "The Behavior of Flip-Flops Used as Synchronizers and Prediction of Their Failure Rate," <u>IEEE Journal of Solid-State Circuits</u> , Vol. SC-15, No. 2					April 1980
	Q	A.D. Singh, "Experiments with an On-Chip IDDQ Current Sensor for VLSI Testing," <u>IEEE Int'l Workshop on IDDQ Testing</u>					1995
EXAMINER				DATE CONSIDERED			
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.							

U.S. Patent and Trademark Office